IFW

Docket No.: 057454-0962 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Hideto HIDAKA	:	Confirmation Number: 4528
Application No.: 10/622,473	:	Group Art Unit: 2824
Filed: July 21, 2003	:	Examiner: Van Thu T Nguyen

For: THIN FILM MAGNETIC MEMORY DEVICE WITH MEMORY CELLS INCLUDING A TUNNEL MAGNETIC RESISTIVE ELEMENT

INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached form PTO-1449. It is respectfully requested that the documents be expressly considered during the prosecution of this application, and that the documents be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

The relevance of **Durlam, M. et al., "Nonvolatile RAM based on magnetic tunnel junction elements" and Scheuerlein, R. et al. , "A 10ns read and write nonvolatile memory array using a magnetic tunnel junction and FET switch in each cell"** is discussed in the

present specification. Each subsequent reference was first cited in an international office action and its relevance discussed therein. A copy of the office action, together with an English language version thereof, is attached for the Examiner's information.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

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INFORMATION DISCLOSURE „CITATION IN AN APPLICATION

(PTO-1449)

ATTY. DOCKET NO.	SERIAL NO.
057454-0962	**10/622,473**
APPLICANT: **Hideto HIDAKA**	
FILING DATE: **July 21, 2003**	GROUP: **2824**

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code2 (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US	6,188,615 B1	02/13/2001	Perner et al.	
		US	6,128,239	10/03/2000	Perner	
		US	6,185,143	02/6/2001	Perner et al.	
		US	5,173,873	12/22/1992	Wu et al.	
		US	2002/0093848 A1	07/18/2002	Thewes et al.	Corresponds to DE 199 14 488 C1
		US	6,349,054 B1	02/19/2002	Hidaka	Corresponds to DE 101 30 829 A1

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Code3 -Number 4 -Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes	Translation No
		EP 1 104 092 A2	05/30/2001	HEWLETT-PACKARD COMPANY, A DELAWARE CORPORATION		X	
		DE 199 14 488 C1	05/31/2000	SIEMENS AG	Corresponds to USP 2002/0093848 A1		X
		DE 101 30 829 A1	07/18/2002	MITSUBISHI DENKI K.K.	Corresponds to 6,349,054 B1		X

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
		Durlam, M. et al., "Nonvolatile RAM based on magnetic tunnel junction elements" IEEE International Solid-State Circuits Conference, 7 to 9 February 2000, pp. 128-129.	
		Scheuerlein, R. et al. , "A 10ns read and write nonvolatile memory array using a magnetic tunnel junction and FET switch in each cell" IEEE International Solid-State Circuits Conference, 7 to 9 February 2000, pp. 128-129.	
		Yamada, K. et al., "A novel sensing scheme for a MRAM with a 5% MR ratio" Symposium on VLSI Circuits, 14 to 16 June 2001, pp. 123-124.	
		Zhang, R. et al., "Windowed MRAM sensing scheme" IEEE International Workshop on Memory and Technology, Design and Testing, 7 to 8 August 2000, pp. 47-55.	
		Kawashima, S. et al.,"A charge-transfer amplifier and an encoded-bus architecture for low-power SRAM's" IEEE Journal of Solid-State Circuits, Vol. 33, No. 5, May 1998, pp. 793-799.	

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.